UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/509,171	05/17/2000	BRIAN JAMES KNIGHT	8479-039	7646

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EXAMINER
BANANKHAH, MAJID A

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/509,171	KNIGHT ET AL.
	Examiner	Art Unit
	Majid A Banankhah	2127

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2000*.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-20* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All   b)☐ Some *   c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>3</u>.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____ .

DETAILED ACTION

1. This office action is in response to application filed on May 17, 2000. Claims 1-20 are considered for examination.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens et al.

(6,272,580) in view of Kopylov (SU, 1837303A1, hereinafter Kopylov).

Claims 1 and	
A CPU, and a plurality of peripheral device	The system of Stevens, Abstract and col. 3, lines 61-67
A CPU having a scheduling controller which includes priority setting means and round robin register means;	CPU is part of the computer and register to note which low priority of peripheral device, col. 1 lines 67 to col. 2, lines 9, col. 3, lines 30-49, and regarding round-robin register see col. 2, lines 24-41,
The priority setting means being associated with each of the peripheral device for setting a selected level,	See Stevens, col. 1, lines 67 to col. 2, lines 9, and Fig. 2, and col. 4, lines 46-49. Stevens teaches of two level of priority ring wherein peripherals devices each have their own priority in each "LP" or "HP" rings.
The round robin register means having marker means for selecting the next one of the peripheral devices to be serviced by the CPU, and also having advancing means for	See, col. 2, lines 24-41, multi-level round-robin arbitration scheme. For advancing means see, Fig. 2. and pointer in col. 3, lines 30-48.

advancing the marker in the round robin register means to a next one of the peripheral devices a highest priority level in the device status register means;	
The peripheral devices each having respective priority setting means for setting the priority level for the respective one of the peripheral devices, depending on the urgency with which that device requires servicing.	Stevens, col. 3, lines 30-48, Temporary elevation register is used to change the priority level for a particular peripheral device. Urgency is associated with priority of the PD.
	While Stevens teaches of priority level (L and H) and priority assigned to each peripherals, he is silent as to "device status register means in which the priority level is set" [step two of the claim]. Kopylov teaches passing of reading bus to a data register and setting the status of level of priorities of requests of PD for the reason to associate a request to a PD. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to assigning status level of priorities in order to be able to associate a request with the proper peripheral device.

Claims 2 and	
A computer system according to claim 1, wherein the device status register means includes a separate device status register for each of the priority levels, and wherein the round robin register means include a plurality of round robin register, a corresponding one of the round robin registers being provided for each of the device status register;	Col. 4, lines 21-37, there are two sets of register, one for the ring and one for each peripheral, which participate, in the round-robin mechanism. There are two rings (round robin register) in Fig. 2. Every round-robin register is associated with a level of priority and consequently associated with device status register (L or H).
Each round robin register containing a single bit;	See col. 3, col. 4, lines 63-68, registers having bit.
The computer system further including priority determination means for identifying a highest priority level devices status register with at least one bit set;	The reference of Stevens teaches of identifying priority level in col. 6, lines 29-40 (multi level round robin priority).

The marker advancing means also including means for advancing the marker in the round robin register means at a highest active priority level.	The pointers in Stevens.
Claims 3	
Wherein different ones of the peripheral devices have different sets of priority levels.	Stevens in col. 4, lines 21-37. Level priority and device priority are different sets.
Claims 4	
Wherein the peripheral devices are communication devices buffers and wherein priority level signals are determined by the state occupation of their buffers.	The system of Stevens can handle any type of communication device including communication device buffer.

Claims 5	
A compute system according to claim 4, wherein some of the peripheral devices, which receive data at a higher rate, may switch to a higher priority level at lower levels of buffer occupancy than others.	Stevens, col. 4, lines 21-37, low priority peripheral device assigned to a high priority ring.
Claim 6	
A compute system according to claim 5, wherein when one of the peripheral devices produces a signal of the appropriate priority level, it may produce signals of lower priority level.	Stevens in col. 4, lines 21-37 teaches of temporary elevation register.
Claim 7	
A computer system according to claim 6, wherein lock-out of the devices is prevented by raising the device priority as servicing becomes more urgent, and once all devices at the highest active priority level are fully serviced, the priority level is dropped to a lower level, and servicing of devices at that level recommences; servicing of devices at the new lower level recommencing at a point where it was left off when a higher priority level up became active.	Stevens, col. 7, lines 35-51, teaches of the functionality behind the high priority and low priority and when there is no high priority dropping to the lower priority level.
Claim 8	
A computer system according to claim 6, wherein the system includes means for	Stevens, col. 1, lines 31-50, in the background teaches of static versus

allocating more system resources to the CPU in response to detection that one or more devices are becoming in need of urgent servicing.	dynamic priority allocation. Round robin is a dynamic resource allocation, therefore, more urgent device uses more resource and can be provided by Stevens's system.

Claims 9	
A computer system according to claim 2, wherein different ones of the peripheral devices have different sets of priority levels	Stevens teaches of different sets of priority in col. 4, lines 21-37, L. P. and H.P. rings and peripheral device priority on each rings.
Claim 10	
A computer system according to claim 9, wherein the peripheral devices are communication devices containing buffers and wherein priority level signals are determined by the state of occupancy of their buffers	Kopylov teaches of state of the status of level of priorities of requests of peripheral devices according to addresses in col. Abstract.
Claim 11	
A computer system according to claim 10, wherein some of the peripheral devices, which receive data at a higher rate, may switch to a higher priority level at lower levels of buffer occupancy than others.	Since priority is assigned to state of occupancy, higher rates can switch to higher switch to higher priority level as well. The system of Stevens does not differentiate between types of priority assigned to peripherals.
Claim 12	
A computer system according to claim 11, wherein when one of the peripheral devices produces a signal of the appropriate priority level, it may produce signals of lower, priority level.	See Stevens, col. 4, lines 21-37, access to elevated low priority is granted before granting access to any of the remaining peripheral devices.

Claim 13	
A computer system according to claim 1, wherein the priority setting means is operable to raise priority of the respective peripheral device, as servicing becomes more urgent, for preventing lockout of the	Stevens in page 7, lines 66-68 to col. 8, lines 19, teaches fully servicing higher priority peripherals if there is no interruption and jumping to a higher priority peripherals once there is an

peripheral device; and wherein the priority setting means is operable to drop the priority level to a lower level once all of the peripheral devices at the highest active priority level are fully serviced, whereby servicing of the peripheral devices at that level recommences; servicing of the peripheral devices at a new lower level recommencing at a point where it was left off when a higher priority level became active.	interruption before servicing of peripherals in sequence. The step of starting servicing of the peripherals when the higher priority is done [in a jump] from a point where it was left is inherent because, without doing so, there will not be priority servicing according to his initial method.
Claim 14	
A computer system according to claim 1, further including means for allocating more system resources to the CPU in response to detection of a state wherein one or more of the peripheral devices are becoming in need of urgent servicing.	Stevens, inherently teaches of allocating system resource to the higher priority peripherals once the need of resource is more, and this is based on the servicing need of the CPU and cannot constitute a patentable limitation.
Claim 15	
A computer system according to claim 4, wherein some of the peripheral devices which have a smaller buffer for receiving data may switch to a higher priority level at lower levels of buffer occupancy than others.	Stevens, col. 4, lines 21-37, if data transfer is being retried to the elevated low priority peripheral devices, that device is granted mastership over other low priority peripheral devices and is of equal priority status to that of the high priority peripheral devices coupled to the high priority ports.

Claims 16	
A computer system according to claim 4, wherein some of the peripheral devices which transmit data at a higher rate may switch to a higher priority level at higher levels of buffer occupancy than others.	Please see the rejection of claim 11.
Claim 17	
A computer system according to claim 4, wherein some of the peripheral devices which have a smaller buffer for transmitting data may switch to a higher priority level at higher levels of buffer occupancy than. others.	See the rejection of claim 15.

Claim 18/20	
A computer system according to claim 10, wherein some of the peripheral devices which have a smaller buffer for receiving data may switch to a higher priority level at lower/higher levels of buffer occupancy than others.	See the rejection of claim 15.
Claim 19	
A computer system according to claim 10, wherein some of the peripheral devices which transmit data at a higher rate may switch to a higher priority levels of buffer occupancy than others.	See the rejection of claim 11.

3.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Majid A. Banankhah** whose voice telephone number is **(703) 308-6903**. A voice mail service is also available at this number.

All response sent to U.S. Mail should be mailed to:

Commissioner of Patent and Trademarks
Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park Two, 2021 Crystal Drive, Arlington. VA, Six Floor (Receptionist). All hand-delivered responses will be handled and entered by the docketing personnel. Please do not hand deliver responses to the Examiner.

All Formal or Official Faxes must be signed and sent to either (703) 308-9051 or (703) 308-9052. Official faxes will be handled and entered by the docketing personnel. The date of entry will correspond to the actual FAX reception date unless that date is a Saturday, Sunday, or a Federal Holiday within the District of Columbia, in which case the official date of receipt will be the next business day. The application file will be promptly forwarded to the Examiner unless the application file must be sent to another area of the office, e.g., Finance Division for fee charging, etc.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is **(703) 305-9600**.

Majid Banankhah

4/4/04

MAJID BANANKHAH
PRIMARY EXAMINER